

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below:

10 APRIL 2006

Jeff Lloyd, Patent Attorney

DECLARATION UNDER 37 CFR §1.132
Examining Group 2812
Patent Application
Docket No. SUN-DA-136T
Serial No. 10/750,252

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner : Richard A. Booth
Art Unit : 2812
Inventor : Chang Hun Han
Serial No. : 10/750,252
Filed : December 31, 2003
Conf. No. : 8844
For : Methods for Fabricating Non-Volatile Memory Devices
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF Lim UNDER 37 CFR §1.132

Sir:

I, Jong-chul Lim, hereby declare:

THAT, I am currently employed by DongbuAnam Semiconductor, Inc., as an Assistant Manager in the Technology Alliance Team. My responsibilities include managing, overseeing and coordinating activities relating to the patent portfolio of DongbuAnam Semiconductor, Inc., including in certain Korean, U.S. and other international patent applications of DongbuAnam Semiconductor, Inc. I have been continuously employed by DongbuAnam Semiconductor, Inc. since November 1, 2005. I received a Master's degree in Chemical Engineering emphasized in Semiconductor Process from San Jose State University in 2004. As one skilled in the art of fabrication of memory devices, I am familiar with the subject matter disclosed and claimed in the above-identified application. I am also familiar with the history of the above-identified

application, including its Korean priority application no. 10-2002-0088281, filed in the Korean Intellectual Property Office on December 31, 2002. I have also reviewed application serial no. 10/750,252, the Office Action dated October 13, 2005, and all references cited therein;

AND, being thus duly qualified, do further declare:

Claims 1-4 and 7-11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Scott (U.S. Patent No. 6,627,524) in view of Pradeep *et al.* (U.S. Patent No. 5,866,448) or Zhou *et al.* (U.S. Patent No. 5,858,847). The Office Action at pages 2-3 states that:

Scott shows the invention substantially as claimed . . . Scott is applied as above but fails to expressly disclose the polymer layers being formed by patterning the sacrificial layer, the polymer layers being generated from the etching of the sacrificial layer . . . Pradeep *et al.* discloses patterning a sacrificial layer (40,42) comprising an oxide and photoresist to form a polymer layer 44 on the sidewalls used to form a gate electrode (see figs. 3-4 and col. 4, lines 18-48). Alternatively, Zhou *et al.* discloses patterning a sacrificial layer (23,24) comprising TEOS oxide in order to form a polymer layer 26 on the sidewalls used to form a gate electrode (see figs. 1-4 and col. 3, line 66 to col. 5, line 53).

The Office Action then concludes, at page 3, that "In view of these disclosures, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Scott so as to form the polymer layers by etching the sacrificial layer because this would reduce the overall number of process steps, thereby decreasing process time."

First, there is no suggestion or motivation that the photoresist of Scott should be replaced with the silicon oxide layer of Pradeep *et al.* or a hard mask layer of Zhou *et al.*, formed using a Tetraethylorthosilicate (TEOS) process. In particular, Pradeep *et al.* discloses a process for forming a lightly doped-drain (LDD) structure where the forming of a polymer sidewall provides the advantage, as described at col. 3, lines 34-36, "that the sidewall oxide deposition onto the silicon active area is eliminated, thereby reducing the risk of channel contamination." This sidewall oxide deposition described in Pradeep *et al.* is not present as a problem in Scott. Zhou *et al.* also discloses a process for forming a LDD structure. Zhou *et al.* describes the need to provide, as stated at col. 3, lines 28-33, "a simpler method of forming the lightly doped drain structure that eliminates the process steps of spacer oxide deposition and spacer etch . . . [t]he

3

Docket No. SUN-DA-136T
Declaration of Jong-chul Lim

width of the polymer layer and the lightly doped drain is highly controllable and can be formed thinner than traditional dielectric and photoresist spacers.” Again, spacer oxide deposition and etch are not present as a problem in Scott. Therefore, neither Pradeep *et al.* nor Zhou *et al.* provide motivation to modify Scott to arrive at the claimed invention.

Second, the method claimed in claim 1 of the subject application does not necessarily reduce the overall number of process steps in Scott. In particular, Scott provides a method of forming at least two programmable read-only memory constructions including the steps of:

1. forming at least one conductive material over a semiconductor substrate;
2. forming at least two patterned photoresist blocks over the conductive material, with a pair of adjacent photoresist blocks being separated by a first gap;
3. forming a coating over the pair of adjacent photoresist blocks and across the first gap between the adjacent blocks;
4. selectively removing the coating from across the first gap while leaving the coating on the pair of adjacent photoresist blocks such that the pair of photoresist blocks and coating remaining on the pair of photoresist blocks define a pair of masking blocs that are separated by a second gap where the second gap is narrower than the first gap
5. using this pattern to etch a pair of spaced floating gate constructions from the conductive material.

(See col. 2, lines 11-24)

Comparing with the method as claimed in claim 1 of:

1. forming an oxide layer and a polysilicon layer on the substrate;
2. forming a sacrificial layer on the polysilicon layer;
3. forming a photoresist pattern on the sacrificial layer;
4. etching a portion of the sacrificial layer through the photoresist pattern, the polymer layers being generated from the etching of the sacrificial layer;

4

Docket No. SUN-DA-136T
Declaration of Jong-chul Lim

5. forming a floating gate and a tunnel oxide using the sacrificial layer and the polymer layers as an etching mask.

It is apparent that on its face, exchanging steps 2, 3, and 4 of Scott with the listed 2, 3, and 4 of subject claim 1 does not reduce the number of steps.

Third, there is no motivation to replace the photoresist layer of Scott with a sacrificial layer of the material discussed in Pradeep *et al.* or Zhou *et al.* because the function of the photoresist layer of Scott does not necessitate a polymer generating characteristic. The photoresist layer of Scott is capable of bonding with a specified coating layer. This coating layer can easily be removed from the areas that have not bonded with the photoresist. (See col. 3, line 48 – col. 4, line 38). Accordingly, there is simply no motivation to modify Scott in the manner suggested in the Office Action.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or of any patent issuing thereon.

Further declarant sayeth naught.

Signed: _____

Date: _____